A 5-Gb/s Decision Circuit Fabricated in a 1.5-μm Super-Self-Aligned Silicon Bipolar IC Technology

R. G. Swartz, V. D. Archer, T. Y. Chiu, Y. Ota, A. M. Voshchenkov, T. Long, K. Moerschel, and W. Possanza

Abstract—**The design and experimental measurements on a clocked decision circuit for optical communication applications are reviewed. The circuit, fabricated in a 1.5-μm super-self-aligned silicon bipolar technology, yields a BER $< 10^{-9}$ at a bit rate of 5 Gb/s. At 2.5 Gb/s, the small signal input data sensitivity is 10 mV, the clock timing margin is 320 ps (288°), the output eye opening is 300 ps (270°), and the rise/fall times are about 100 ps.**

I. Introduction

SILICON bipolar integrated circuit technologies have enjoyed a recent rise in popularity for very high performance applications, including lightwave [1]. Leading this resurgence have been the advanced bipolar processes collectively referred to as "double-poly" technologies. The most highly optimized of these are the so-called "super-self-aligned" IC processes that use polysilicon contacts, precisely controlled thin film deposition and etching techniques, and self-aligned silicidation ("salicides") to achieve many levels of maskless feature alignment. These result in a considerable reduction of the parasitic capacitances and resistances that ordinarily limit the circuit performance of conventionally fabricated devices. For the work described in this letter, we employed a fully super-self-aligned bipolar silicon technology with 1.5-μm features (Fig. 1) that achieves circuit performance comparable to conventional sub-micron processes [2]–[4].

This paper reviews measured results for a clocked decision circuit intended for optical communication applications. Circuit goals during the design stage included clocking at the maximum possible bit rate, with sensitivity better than 50 mV at 2.5 Gb/s and a corresponding clock phase margin of at least 180°. The desired output rise/fall times were on the order of 100 ps.

II. Circuit Configuration

The circuit, Fig. 2, consists of a central master/slave flipflop composed of two *D*-latches. The *D*-latches are conventional ECL circuits with differential, current steering logic and single stage emitter followers. The transistors have emitter dimensions of 10 μm × 1.5 μm, a nominal f_T of 12 GHz, and operate at a peak current density of 135 $\mu A/\mu m^2$. Power dissipation per latch is 30 mW, giving a total flipflop P_D of 60 mW. Clock and data are buffered by circuits consisting of emitter follower level shifters and an ECL differential pair/follower stage. Design values for the loaded small signal gain and −3 dB bandwidth are 16 dB and 2.4 GHz, respectively. Power dissipation is 155 mW and 105 mW, respectively, for the clock and data buffers. The output buffer consists of three ECL stages with the final stage having collector outputs internally terminated by 50 ohms to ground. Nominal power dissipation in this buffer is 370 mW, and the buffer's bias control lead is brought off chip for adjustment of the output swing.

Although a fully differential ECL logic configuration is used throughout the design, ECL logic levels are not used for input/output. The V_{TT} (−2 V) supply used by conventional ECL was eliminated at a cost of somewhat increased power supply dissipation. Collector outputs are used to provide added circuit stability. Inputs are self-biased to allow ac-coupled clock and data; and the outputs will drive a grounded load directly. Low-level signal swings (250 mV single-ended, 500 mV differential) are used everywhere for high speed except at the output.

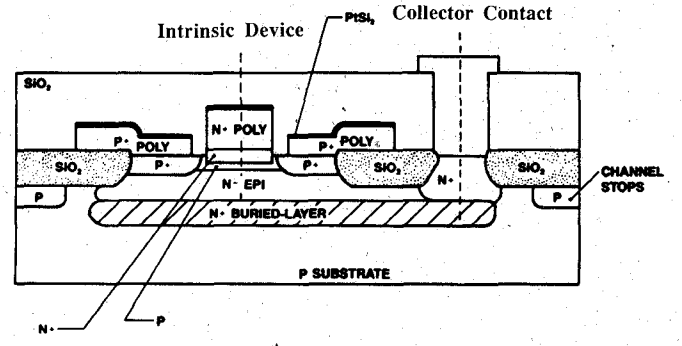

Fig. 1. Cross-section diagram of bipolar device. Intrinsic device is defined by a polysilicon contact to the N^+ emitter that is located above the *P*-type intrinsic base and *N*-type collector. A 200 nm SiO_2 spacer separates the salicided emitter and P^+ extrinsic base poly contacts. Only one critical alignment is required to define emitter, extrinsic base, emitter, and base contacts. This super-self alignment results in reduced base-collector and collector-substrate capacitance, and lowered emitter and extrinsic base resistance.

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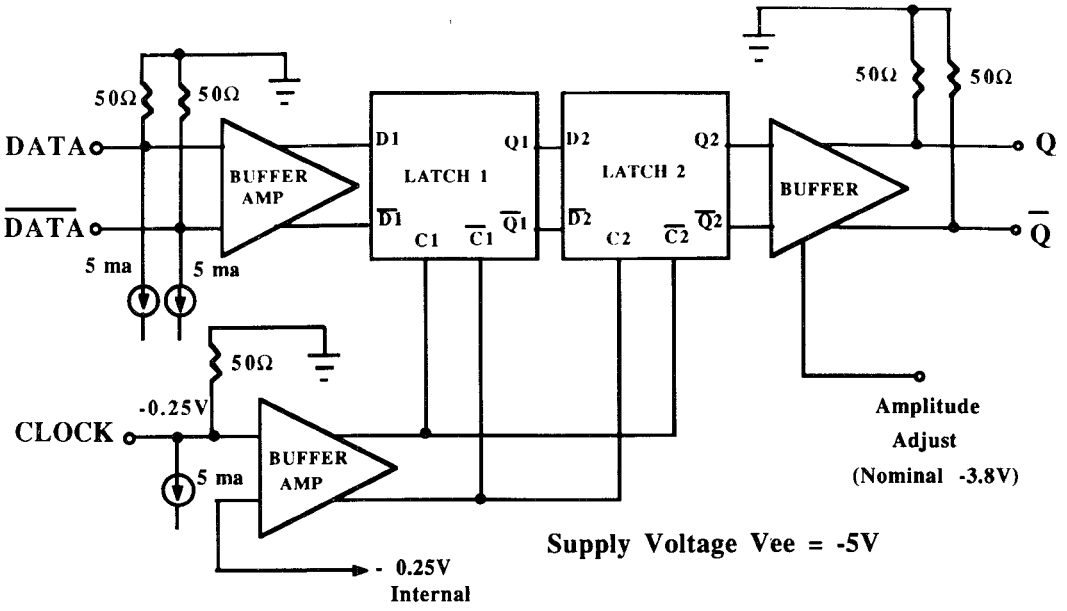
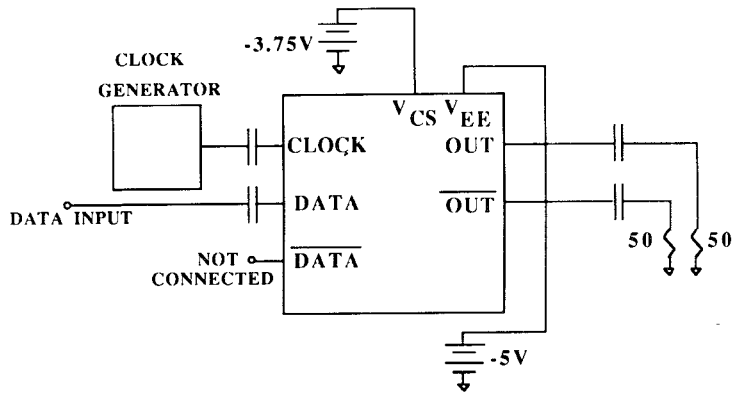
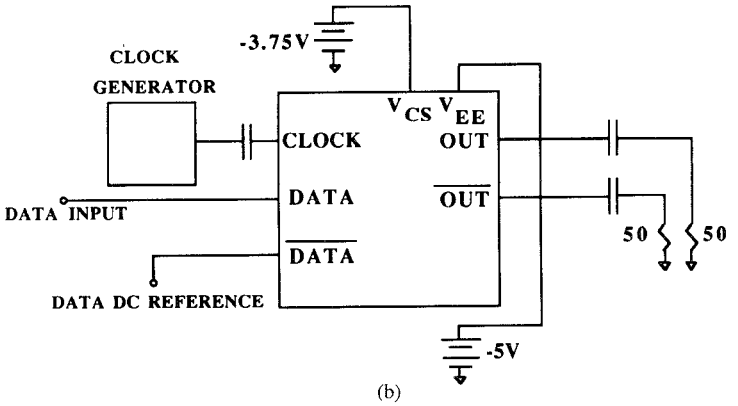


Fig. 2. Block diagram of clocked decision circuit.



(a)



(b)

Fig. 3. Decision circuit test configurations. Outputs are shown ac-coupled to external 50 ohm loads, but circuit will drive grounded loads directly. Inputs are internally terminated in 50 ohms to ground. Output drive is set by V_{CS} terminal (-3.75 V gives 600 mV output swing into 50 ohm load). (a) AC-coupled data input. Data reference is not used This is the easiest configuration to use, but does not give best sensitivity because of offsets. (b) DC-coupled data input for maximum data sensitivity.

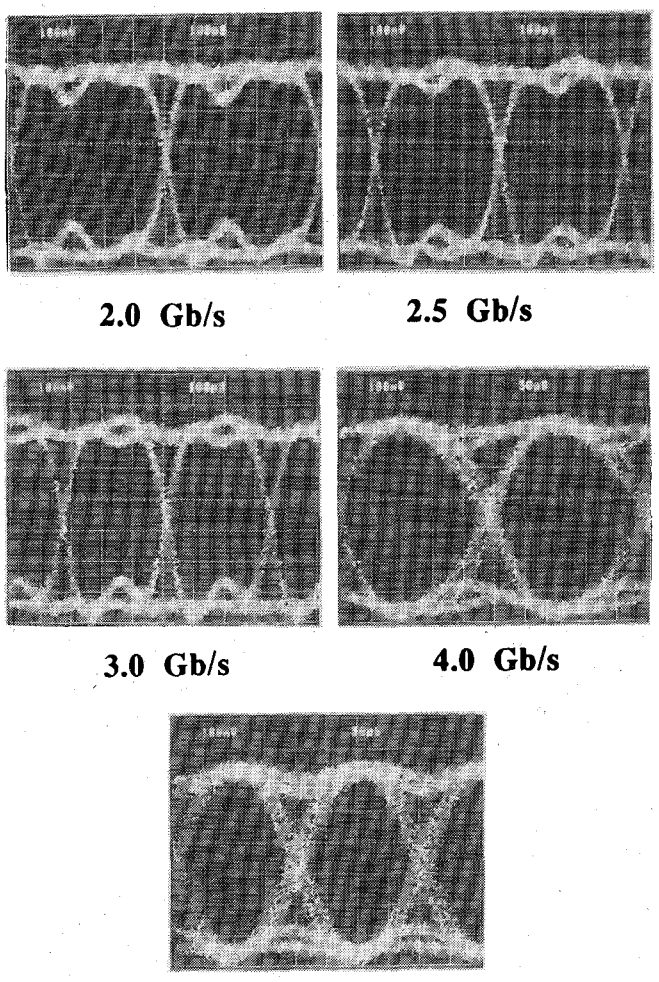


Fig. 4. Output eye diagrams at 2.0 Gb/s, 2.5 Gb/s, 3.0 Gb/s, 4.0 Gb/s, and 5.0 Gb/s.

III. Measurements

Circuit measurements were made on-wafer using microwave probes, and also on chips mounted on ceramic substrates with external bypassing of dc supply and bias nodes. The test circuit configurations are shown in Fig. 3. Two test configurations were used that differed in the manner in which the data signal was supplied to the test chip. In Fig. 3(a), the data signal is ac-coupled to the circuit and on-chip bias generators are used to set the proper dc levels at the data inputs to the circuit. This configuration is the most convenient to use, but does not give the maximum input sensitivity. In Fig. 3(b), the data signal is dc-coupled to the circuit at a fixed dc bias, externally applied, and the data reference input is set by an adjustable external bias to maximize circuit sensitivity. In both cases, a 500 mV peak-to-peak clock signal is applied single-ended, ac-coupled. A 5 Gb/s pulse pattern generator and error detector were used for bit-error rate (BER) measurements. In all cases, the data signal applied was a non-return-to-zero $2^{23} - 1$ pseudorandom code with an error threshold defined as 10^{-9}. The supply voltage was fixed at -5V, and the output amplitude was adjusted to give a nominal 600 mV swing peak-to-peak. Under these conditions, the supply current was approximately 160 mA,

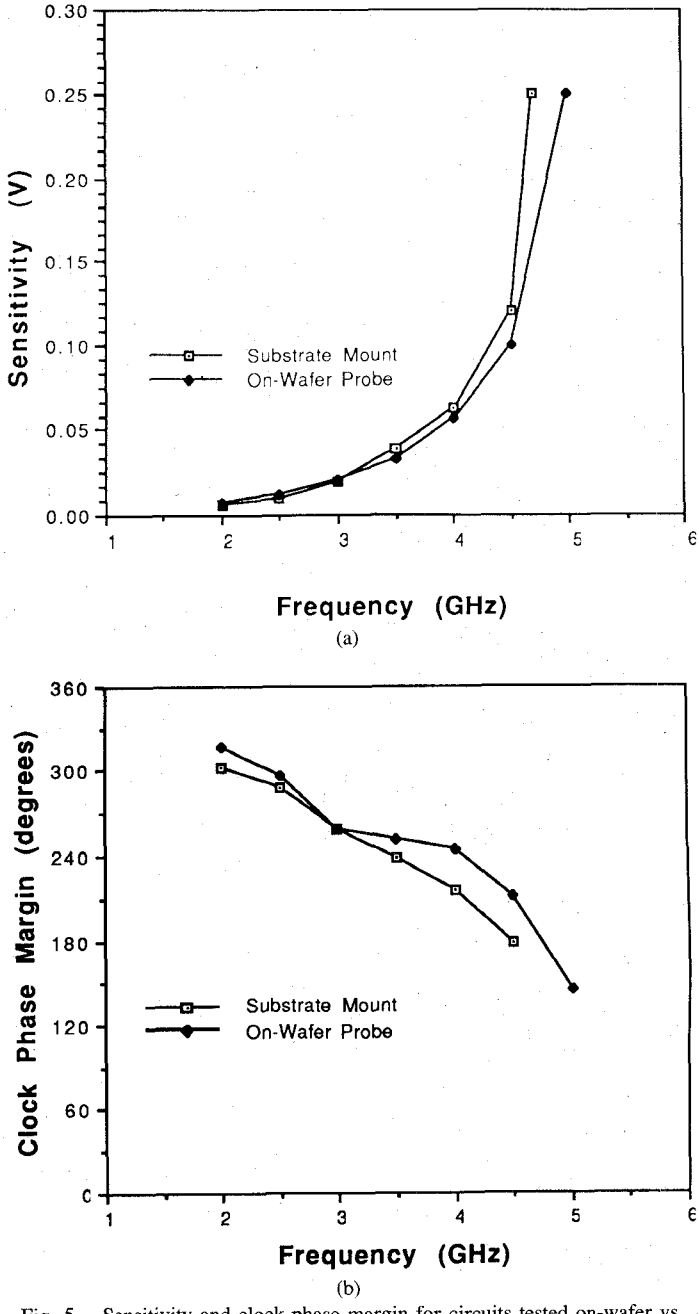


Fig. 5. Sensitivity and clock phase margin for circuits tested on-wafer vs. ceramic-mounted chips. (a) Sensitivity. (b) Clock phase margin.

giving a power dissipation of 800 mW. For initial wafer mapping, devices were marked as pass/fail depending on their ability to demonstrate 50 mV sensitivity at 3.0 Gb/s with an ac-coupled data input signal (configuration Fig. 3(a)). Operation at 5.0 Gb/s with a BER $< 10^{-9}$ was observed, although at a relatively high input signal level in most cases ($>$ 250 mV data input). Fig. 4 shows output eye diagrams at data rates ranging from 2.0 Gb/s to 5.0 Gb/s. The nominal 10%–90% rise times ranged from 95 ps to 104 ps (60 ps–70 ps, 20%–80%), while the corresponding fall times were 95 ps to 110 ps (62 ps–80 ps, 20%–80%).

Fig. 5 shows sensitivity and clock phase margin plotted vs. frequency for decision circuits probed on-wafer versus mounted on the ceramic substrates. The dc-coupled data input (Fig. 3(b)) test configuration was used. In both cases,

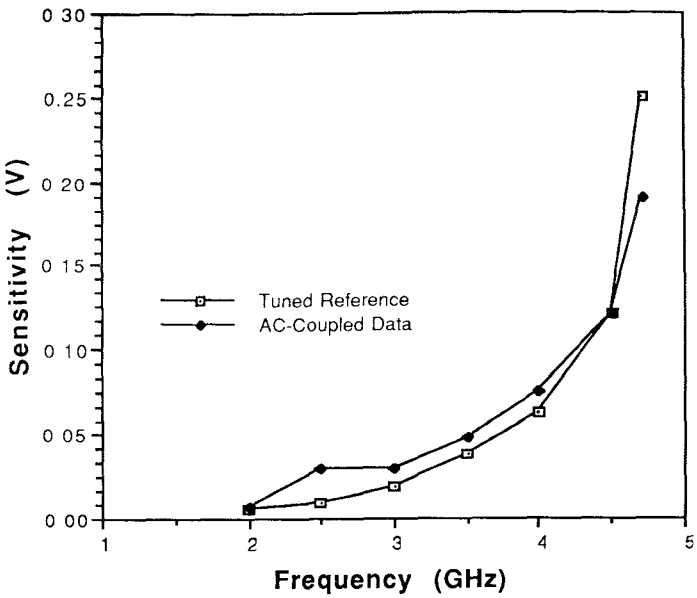


Fig. 6. Effect of dc reference tuning on data input sensitivity.

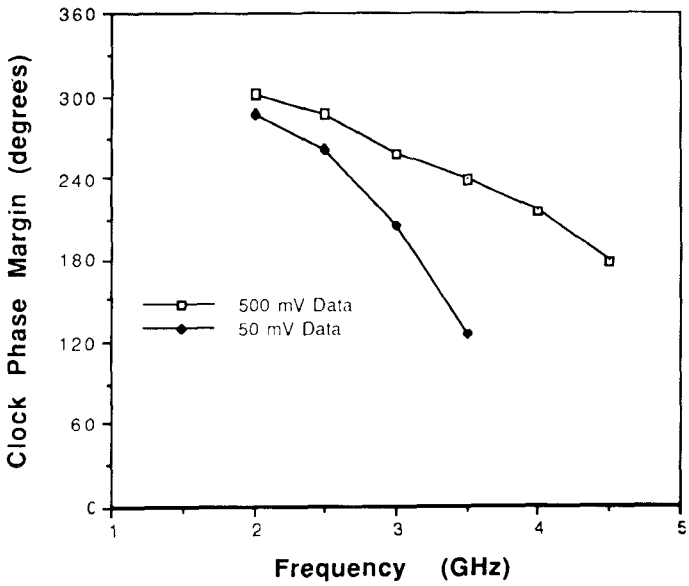


Fig. 7. Clock phase margin for large (500 mV) and small (50 mV) data inputs.

sensitivity is approximately 10 mV at 2.5 Gb/s, and the corresponding clock phase margin approaches 300°. Some slight performance degradation in sensitivity and phase margin is observed at higher bit rates for the mounted chip as compared to the wafer test, and the maximum bit rate decreased from 5.0 Gb/s to 4.7 Gb/s. This loss in performance is attributed to chip heating. Fig. 6 shows plots of decision circuit sensitivity vs. bit rate for a ceramic-mounted chip using ac-coupled input data (Fig. 3(a)) and dc-coupled, reference adjusted input data (Fig. 3(b)). Improved sensitivity is obtained, particularly at lower bit rates when the data reference is adjusted to optimize sensitivity. This particular measurement depends on the dc-offset level of the particular circuit measured.

Fig. 7 shows plots of clock phase margin vs. bit rate for a ceramic-mounted chip under 500 mV peak-to-peak data input, and 50 mV peak-to-peak data input conditions. We believe that the smaller amplitude data measurement may more accurately reflect the performance of this circuit in a real world application where eye closure is present due to inter-symbol interference. In the large signal data input case (the conventional measurement method), the clock phase margin exceeds 180° at data rates up to and over 4 Gb/s. In the case of a small signal data input, 180° phase margin is maintained only to a little over 3 Gb/s. Fig. 8 shows a similar measurement of output eye opening vs. bit rate, again for large and small signal data input conditions. Clock phase margin and output eye opening measurements were repeated at power supply voltages of −4.5 V, −5.0 V, and −5.5 V using 50 mV data input. Measurements were identical to those reported in Figs. 7 and 8, independent of supply voltage, within a margin of ±10 ps. Chip performance across temperature is yet to be characterized, although we have observed some reduction in sensitivity at 80°C.

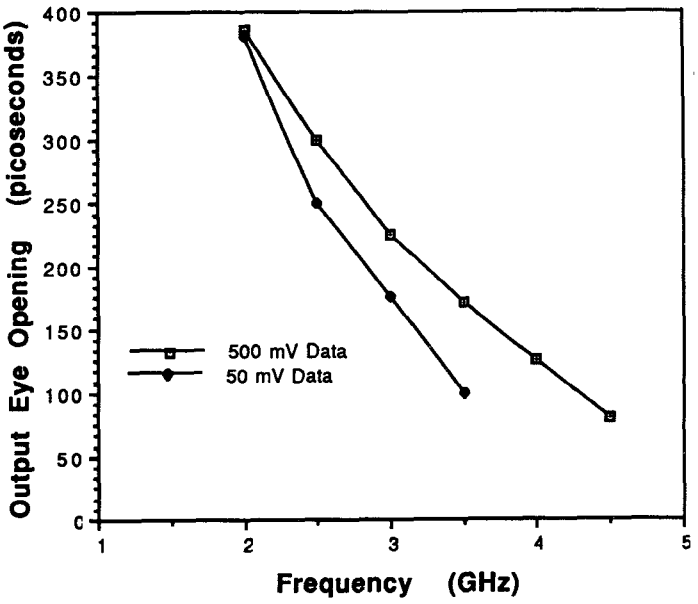


Fig. 8. Output eye opening for large (500 mV) and small (50 mV) data inputs.

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